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TERAFLUX: Harnessing dataflow in next generation teradevices

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ABSTRACT

The improvements in semiconductor technologies are gradually enabling extreme-scale systems such as teradevices (i.e., chips composed by 1000 billion of transistors), most likely by 2020. Three major challenges have been identified: programmability, manageable architecture design, and reliability. TERAFLUX is a Future and Emerging Technology (FET) large-scale project funded by the European Union, which addresses such challenges at once by leveraging the dataflow principles. This paper presents an overview of the research carried out by the TERAFLUX partners and some preliminary results. Our platform comprises 1000+ general purpose cores per chip in order to properly explore the above challenges. An architectural template has been proposed and applications have been ported to the platform. Programming models, compilation tools, and reliability techniques have been developed. The evaluation is carried out by leveraging on modifications of the HP-Labs COTSon simulator.

1. Introduction

Silicon manufacturing technologies, such as FinFET [1] transistors and 3D-die stacking [2] that are currently available, will allow new chips (that we call teradevices) with a huge number of transistors (for current ITRS [3] projections, 1 Tera or 10^{12} transistors), therefore opening the doors to the possibility of exploiting the extremely large amount of parallelism in different ways. It is expected that such systems will be able to perform at least one Exa-FLOPS or 10^{18} floating-point operations per second.

In such future exascale machines, the number of general purpose cores (i.e., compute elements) per die will exceed those of current systems by far. This suggests a major change in the software layers that are responsible of using all such cores. The three

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major challenges: programmability, reliability and complexity of design are here briefly introduced. Also, a new Program eXecution Model [4–6] seems suited in order to address such challenges.

Given the large number of transistors and the diversity in the requirements for different applications, it is natural to expect that these massively parallel (or concurrent teradevice) systems will be composed of heterogeneous cores. Thus, programmability of such large-scale systems will be a major challenge. Moreover, such large systems are expected to become more and more susceptible to failures, due to the increasing sensibility to process variations and manufacturing defects. Thus, this extreme scale of device integration represents a second major concern, in terms of reliability, for future many-core systems. Finally, the software industry is lagging behind as general purpose applications cannot take advantage of more than a handful number of cores compared to the larger degree of parallelism offered by the current and future processors. Starting from this premise, there is the need for new ways to exploit the large parallelism offered by future architectures as expected to be a reality beyond the year 2020.

The dataflow concept is known to overcome the limitations of the traditional control-flow model by exploring the maximum parallelism and reducing the synchronization overhead. As recalled by Jack Dennis [7], dataflow is "A Scheme of Computation in which an activity is initiated by presence of the data it needs to perform its function". The dataflow paradigm is not new, but recently it has met mature silicon technology and architectural models to take advantage from the large intrinsic parallelism.

TERAFLUX [8] is a Future Emerging Technologies (FET) large-scale project funded by the European Union. The aim is to exploit the dataflow paradigm in order to address the three major challenges presented above (i.e., programmability, reliability, and manageable architecture design). Since we are targeting 1000+ core systems, the dataflow paradigm enables us to use the increased degree of parallelism which emerges in future teradevices.

The rest of the paper is organized as follows. Section 2 provides a general overview of the project. Remaining sections are focused on describing the concepts together with the major achievements resulting from our research activity. In particular, Section 3 describes possible applications based on the OmpSs programming model, while Section 4 details a further possibility of using a productivity language such as Scala thanks to a dataflow runtime called DFScala. Another common layer (OpenStream, presented in Section 5) is used for mapping feed-forward dataflow into lower-level dataflow threads as expressed by the T∗ Instruction Set Extension, described in Section 6, together with the architecture of our target system. Section 7 describes the Fault Detection Units (FDUs), which provide fault detection management through monitoring techniques and redundant execution of dataflow threads. The experiments are integrated into a common simulator based on the HPLabs COTSon [9] , presented in Section 8. Finally, Section 9 introduces the codelet model, while Section 10 concludes the paper.

2. General overview of the TERAFLUX project

To investigate our concepts, we use dataflow principles at any level of a complete transformation hierarchy, starting from general complex applications (able to load properly a teradevice system) through programming models, compilation tools, reliability techniques and architecture. Fig. 1 shows the TERAFLUX layered approach.

Different layers allow to transform application source code into a dataflow-style binary, and to execute it on the target architecture (which is at the current moment based on off-the-shelf cores like x86_64, even if our approach is Instruction Set agnostic—see Section 8 for more details). The top level of this hierarchy is represented by real world applications, which allow us to stress

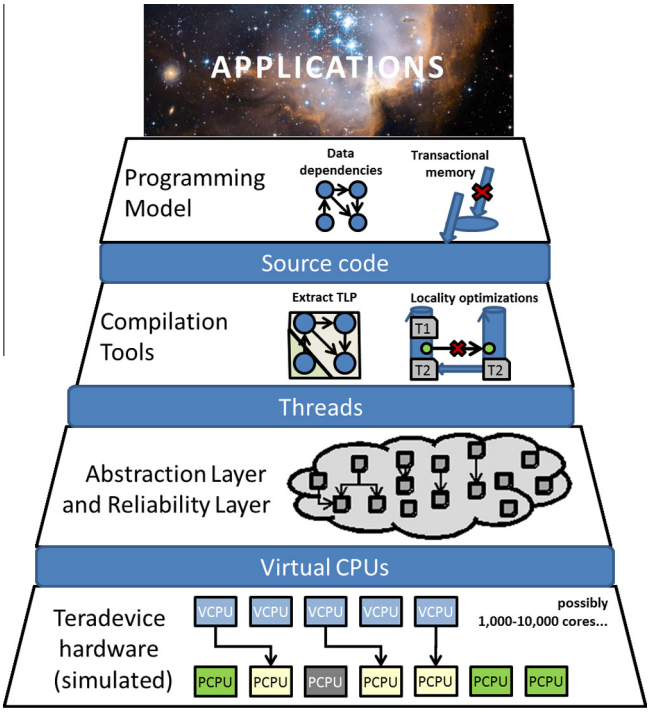

Fig. 1. The TERAFLUX transformation hierarchy.

the underlying teradevice hardware. In the TERAFLUX project, implicit parallelism refers to the set of constraints on the concurrent execution of threads, and the expression of these constraints in the source code. These constraints can be dependencies, atomic transactions, synchronization barriers, privatization attributes, memory layout and extent properties, and a wide variety of hints. An explicitly parallel program, on the other hand, is made of concurrency constructs making the thread creation, termination, and possibly some target-specific aspects of the execution explicit [10–12].

A dataflow oriented programming model allows expressing data dependencies among the concurrent tasks of an application. Such concurrent tasks can be subdivided even more—at lower levels—into *DataFlow Threads* (or *DF-Threads*), also simply referred as threads when clear from the context. Nevertheless, applications use large data structures with in-place updates, for efficient memory management [13–15] and copy avoidance. Such applications may require a mechanism to express the non-interference of concurrent updates to shared data. To meet such need, we selected Transactional Memory (TM), as the most promising programming construct and concurrency mechanism for specifying more general forms of synchronization among threads, while preserving the composability of parallel dataflow programs and promising a high level of scalability [16]. We achieve this by defining a specific layer for studying the integration between the TM and dataflow programming models [17–19].

Besides the programming model, implicit parallelism must be exploited by a compilation tool-chain [20–22], being able to convert dependencies and transactions, into scalable target-specific parallelism. It is also responsible for properly managing the inter-node communications and a novel memory model. Compiler effectiveness is guaranteed by the implementation of a generalization of the state-of-the-art algorithms to expose fine-grained dataflow threads from task-parallel OpenMP-, StarSs- or HMPP-annotated [23,24] programs. The algorithm generalization leverages a new dependence-removal technique to avoid the artificial synchronizations induced by in-place updates in the source program [25,26].

Our goals in designing an efficient compilation tool-chain are to capture the important data reuse patterns, to optimize locality and

reduce communication bandwidth, and to provide compiler support for transaction semantics embedded into a dataflow programming model, such as OpenStream [27]. Both productivity and efficiency programming layers are supported. Compiler directives are used to lower the abstraction penalty of the productivity layer, and to explicitly exploit parallelism and locality.

As mentioned in the Section 1 reliability will be a major concern for future many-cores architectures. With the aim of limiting the impact of faults in the target architecture, dedicated hardware modules are devoted to monitor the health of the system, and drive specific counteractive measures [28,29]. To achieve this goal in TERAFLUX, we focused on inter-core fault detection techniques using Fault Detection Units (FDUs) [30]. We considered different FDU variants (push, pull, alert mechanisms for heartbeat messages), FDU implementations, and interfaces.

We propose a functional FDU specification based on the MAPE (Monitoring, Analysis, Planning, and Execution) [31] cycle. Abstract message interfaces of the FDU to all communication units (e.g., FDU-core, FDU-operating system, etc.) were specified for push, pull, and alert messages. Core health is monitored by exploiting currently available performance monitoring and machine check hardware features (e.g., machine check architecture of current AMD/Intel processor families).

System resources are managed at the highest level by the operating system. The main objective of the operating system is to balance the workload among the nodes while keeping an acceptable level of fault tolerance. The control of scheduling and the resource managing are hierarchically performed: distributed FDUs are used to guarantee the characteristics of the basic nodes by accessing the different resources such as the cores, and local memories. Similarly to the FDU, the other resources of the TERAFLUX system are hierarchically organized, mainly resembled to a set of nodes interconnected with each other. Each node contains hardware structures for scheduling the medium/fine-grain dataflow threads (TSUs or Thread Scheduling Units) generated by the compilation tool-chain, and execute them.

The TERAFLUX architecture is designed in order to support the programming and execution models developed by the higher level layers. At this point the project focuses on defining the basic architecture modules as well as the necessary instruction extensions to support the programming and execution model. The basic architecture consists of a number of multi-core nodes. We are ISA agnostic, in principle, but we wanted to demonstrate our concept with a well-known ISA such as the x86_64. The nodes are interconnected through a Network on Chip (NoC). TERAFLUX supports a global address space across the whole system. For producer-consumer patterns, there is no need for traditional coherency because the dataflow model is based on the single assignment semantics. Different memory types (e.g. shared and non-shared) are defined as to store particular data and metadata of the programs, while non-determinism in accessing the shared data is guaranteed through transactions.

The aim of the lowest layer of the TERAFLUX hierarchical approach is to the provide software and hardware infrastructures capable of simulating all the modules composing the target system. For the simulation and evaluation of the system we chose a state of the art many-core simulation infrastructure (HPLabs COTSon [9]), which is able to scale up the number of cores to two orders of magnitudes larger than what is currently available. This simulation infrastructure represents a common point for all the partners, allowing them to test their research ideas and integrating them in a common platform.

3. Leveraging dataflow through the task-based approach

One of the key aspects of the TERAFLUX project is the proposal of a new programming and execution model [32–34] based on dataflow instead of the traditional control-flow paradigm. Dataflow is known to overcome the limitations of the traditional control-flow model by exploring the maximum parallelism and reducing the synchronization overhead. We leverage such dataflow principle with the combination of OpenStream [27] and StarSs/OmpSs [10–12].

OpenStream compiler — GCC based — is an entry point to TERAFLUX compilation toolchain: applications parallelized with TERAFLUX programming models need to be translated manually or automatically to code annotated with OpenStream directives. We use StarSs memory regions [35] as a case study for translation to OpenStream. OpenStream and StarSs have different features with regard to how data used for computation are represented and how data dependencies are handled:

- OpenStream's basic unit of computation is a *dataflow stream* whereas StarSs applications use *dynamic memory regions* specified by the programmer for communication between tasks
- OpenStream requires explicit task dependencies to maintain correctness of parallel execution whereas data dependencies of StarSs tasks are inferred at runtime.

The comparison shows that translation, when manually done, requires the programmer to identify data dependencies between StarSs tasks and express them with OpenStream streaming constructs. As it is stated in [27], the idea behind StarSs-OpenStream translation scheme is to encode StarSs memory regions as a set of streams that contain versions of memory locations accessed by tasks. The most recent versions in the set of streams are calculated by modified StarSs dependence resolver, and determine live data identified by StarSs memory regions at the given point of application execution. The set of streams is attached to each OpenStream task, and is used by OpenStream runtime to determine data dependencies between tasks and to synchronize concurrent memory accesses. Detailed explanation of the translation scheme and proof of correctness of the algorithm is found in [27].

A source-to-source translator is being developed that carries out StarSs-OpenStream translation at compile time. The key components of the translator are a parser that parses StarSs pragmas to identify memory regions and their directionalities further used to calculate their live versions, and a code generator that generates call expressions to aforementioned StarSs dependence resolver. The code generator also generates OpenStream task pragmas with the set of version streams. Generated code is further passed to OpenStream compiler. A prototype version of this translator is publicly available and has been tested with some sample applications. It can be downloaded from http://openstream.info website.

The StarSs programming model [35] provides a paradigm for the development of applications following the sequential programming paradigm but based on an execution model that exploits the inherent concurrency of the applications taking into account the existing data dependencies. The code is developed in a standard, sequential language, such as C or FORTRAN. On the users side there are no explicit parallel constructs, like in thread or stream models.

Since the paradigm is task-based, the programmer needs to add annotations or compiler directives to the code to mark those pieces of code which are to be considered a task and the directionality of key arguments of the tasks. At runtime, this information about the directionality of the task data is used to build a task data-dependence graph that exhibits the inherent data dependencies of the application as well as its potential task parallelism. Recently, an extention of OpenMP was proposed. OmpSs [36,37] is an implementation of StarSs which extends

the OpenMP explicit tasks [38] with dependence clauses that indicate the directionality of the tasks arguments, and on the Task Superscalar design [39,40].

Fig. 2 shows an example of OmpSs code. The example implements a Cholesky factorization. The kernels of the factorization have been annotated with OmpSs compiler directives. The directionality clauses (`input`, `output`, `inout`) indicate whether the given parameter is read, write or read and write in the scope of the task.

Within the framework of TERAFLUX, OmpSs has been used as a high level programming model to develop applications. The OmpSs coarse-grained tasks are then translated to finer dataflow threads that are executed in the dataflow architecture. OmpSs is available as open source and can be downloaded from http://pm.bsc.es/ompss website.

3.1. Parallel Updates in StarSs/OmpSs

Although independent tasks from the dependence graph are scheduled for execution, StarSs also provides annotations for simultaneous updates to memory locations shared by multiple tasks. The programmer is responsible to protect such parallel updates. StarSs provides a lock-based synchronization mechanism for concurrency control, and to deal with such concurrent updates. But the use of locks opens the door to deadlock, livelock, nondeterminism, and lost compositionality.

In order to avoid such problems, Software Transactional Memory (STM), an alternative method to lock based synchronization has been used to access shared memory locations. TinySTM [41,42], a lightweight STM library has been integrated into the StarSs framework with this purpose. Instead of introducing a new pragma into the StarSs framework, the implementation of the existing lock pragma was modified to generate transactions which update the shared memory locations. When a lock pragma is encountered StarSs starts a transaction and saves the stack context. If the transaction encounters a conflict at a later stage in the execution then the saved stack context is used to restart the transaction. The critical memory location which is being updated is then loaded into a local variable using TinySTM library calls. The updates are performed on this local copy. At the end the value in this local copy is stored back to the main memory location shared between tasks. In case of a conflict the transaction is restarted from the point where the stack context has been saved. In case of no conflicts the transaction is committed and the results made permanent.

The idea of optimistic STM based synchronization versus pessimistic lock based concurrency control has been tested on applications where parallel updates are performed on memory locations by tasks. The results prove that we obtain higher performance with STM in applications with high lock contention. The overhead of using STM is in the aborts and restarts of transactions in case of a conflict. Hence an analysis has been performed on the time spent by transactions in rollbacks. The results [18] show that in cases where lock based synchronization performs better than STM, the overhead incurred due to rollbacks play a major role. Analysis has been also done on executing longer transactions versus smaller transactions. The trade-off is to create multiple smaller transactions and thus spend more time in start and commit of transactions versus longer transactions and hence longer time in rollbacks in case of a conflict [18].

4. DFScala: constructing and executing dataflow graphs

One part of this project is the construction of a high level dataflow framework which serves two purposes: Overall goals of TERAFLUX included: (i) to provide a high productivity language in which to construct dataflow programs, and (ii) to provide a high level platform for experimenting with new ideas such as using the type system to enforce different properties of the dataflow graph and different memory models. With these goals in mind, we constructed a high level dataflow framework called DFScala.

DFScala provides a key foundation and implements the base functionality of this research platform. One distinguishing feature of DFScala is the static checking of the dynamically constructed DF graph.

In a dataflow program the computation is split into sections. Depending on the granularity of the program these vary from a single instruction to whole functions which can include calls to other functions, allowing arbitrarily large computation units. All of these sections are deterministically based on their input and side-effect

```
#pragma omp task inout ([TS][TS]A)
void spotrf (float *A);
#pragma omp task input ([TS][TS]T) input ([TS][TS]B)
void strsm (float *T, float *B);
#pragma omp task input ([TS][TS]A,[TS][TS]B) inout ([TS][TS]C )
void sgemm (float *A, float *B, float *C);
#pragma omp task input ([TS][TS]A) inout ([TS][TS]C)
void ssyrk (float *A, float *C);

void cholesky(float *A) {
    int i, j, k;
    for (k=0; k<NT; k++) {
        spotrf(A[k*NT+k]) ;
        for (i=k+1; i<NT; i++)
                strsm(A[k*NT+k], A[k*NT+i]);
        for (i=k+1; i<NT; i++) {
            for (j=k+1; j<i; j++)
                sgemm(A[k*NT+i], A[k*NT+j], A[j*NT+i]);
            ssyrk(A[k*NT+i], A[i*NT+i]);
        }
    }
}
```

Fig. 2. Example of code annotated with OmpSs compiler directive.

free. The execution of the program is then orchestrated through the construction of a directed acyclic graph where the nodes are the sections of computation and the vertices are the data dependencies among these. An example of this can be seen in Fig. 3. Once all the inputs of a node in the graph have been computed the node can be scheduled for execution.

The DFScala library is open source and provides the functionality to construct and execute DF graphs in Scala. The nodes in the graph are dynamically constructed over the course of a program and each node executes a function which is passed as an argument. The arcs between nodes are all statically typed. More details are in recent works [43–45]. DFScala is available at http://apt.cs.man.ac.uk/projects/TERAFLUX/DFScala website.

4.1. Combining dataflow and transactional memory

Transactional memory and dataflow are a good combination of paradigms because of transactions isolation. The detection of conflict and possible retrying is taken care of wholly by the underlying system. As far as the user code is concerned a particular thread sees no evidence of interaction with any other thread, other than a possible increase in execution time. This isolation leads to specific coherency and data dependency properties that fit very well with dataflow programming.

4.2. Coherency

The isolation properties of transactional memory ensure that state updates only become visible at the point that a transaction commits. This means that, unlike with shared state and locks, the coherence model is the same for a transaction as it is for a node of a dataflow computation. As such a transaction can be treated by the memory model as a distinct node of a dataflow graph, so the addition of state does not require a fine grained understanding of the interleaving of operation by the programmer, or strengthening the coherency model in the hardware. A graphical example of this effect can be seen in Fig. 4.

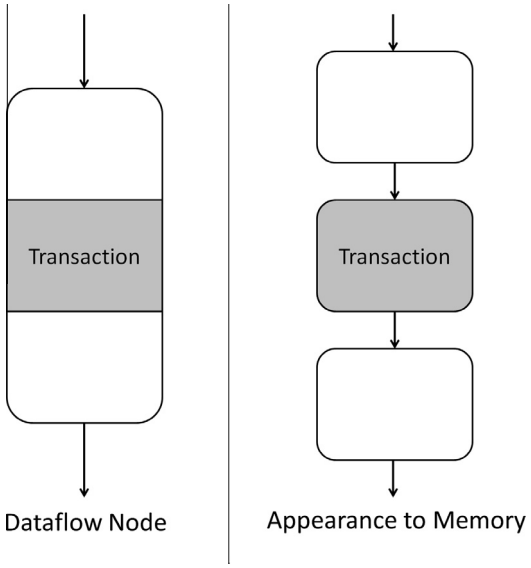

Fig. 4. On the left a node in the dataflow graph containing a transaction, on the right how this can be viewed as three nodes by the memory system.

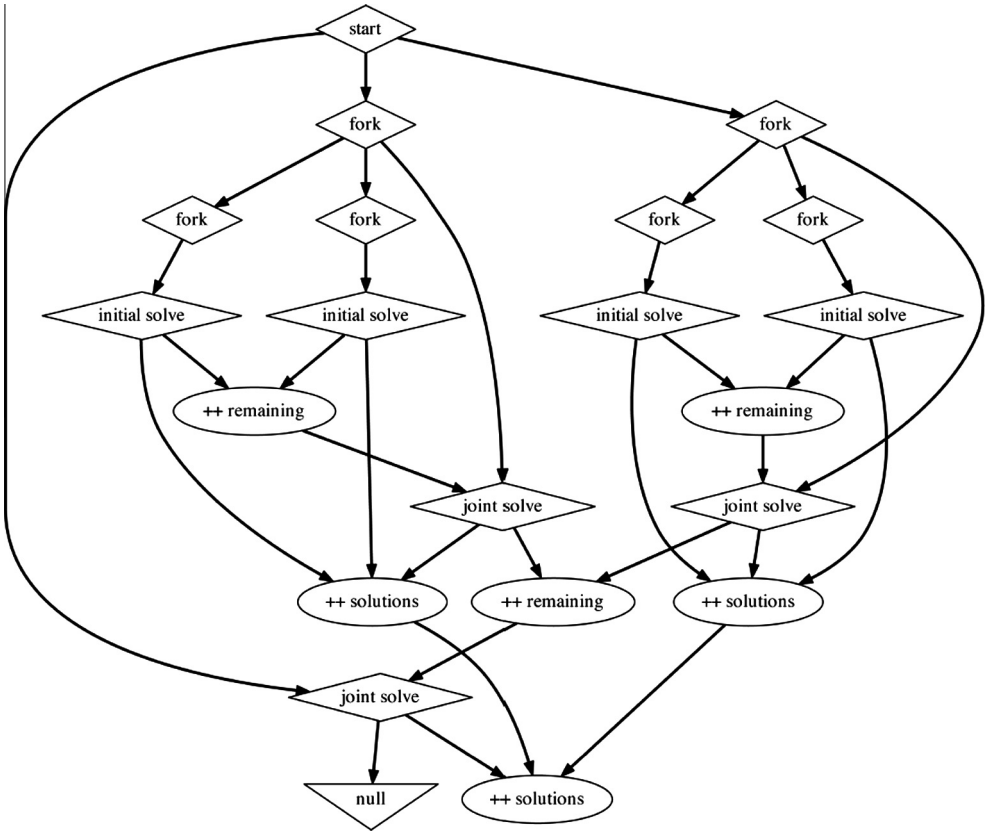

Fig. 3. An instance of a dataflow graph for a circuit routing algorithm.

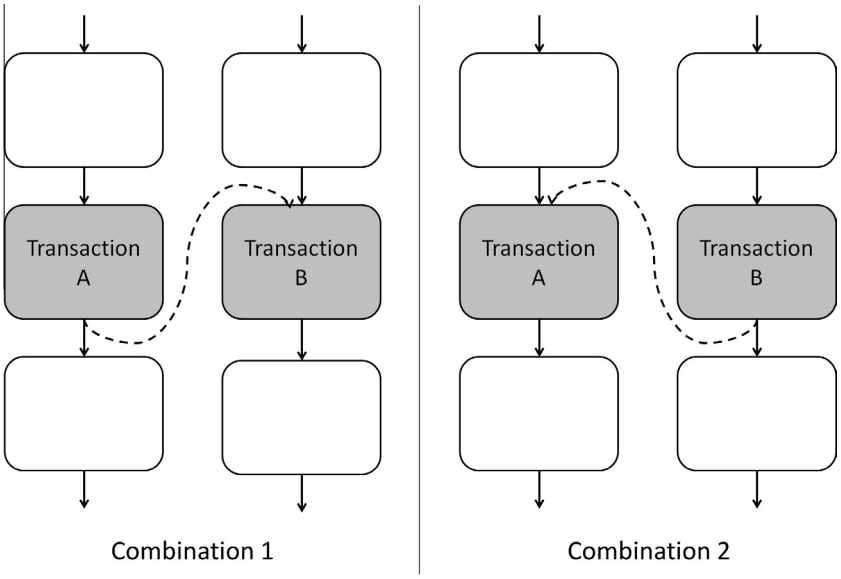

Fig. 5. The two possible formulations of a section of the dataflow graph containing two conflicting transactions. The dashed data dependency will be inserted and enforced at runtime by the transactional memory system, making the relationship between transactions part of the dataflow graph.

4.3. Data dependencies

Isolation also means that transactions can be viewed as dataflow tasks whose data dependencies are determined as the program executes. This is possible because for any two transactions that access the same state and at least one transaction modifies it, they will appear to execute serially. Effectively the TM is adding a dependency to the dataflow graph at runtime. An example of this can be seen in Fig. 5.

The combination of these two features means that transactions can be viewed as nodes in the dataflow graph. This means that we are now describing a family of dataflow graphs which maintain dataflow semantics instead of the weakened dataflow graphs provided by lock based solutions. As such, this combination is deadlock free, like a pure dataflow graph and offers a far smaller number of possible execution paths. This makes it far less invasive to the correctness of the dataflow model while still providing a clean and efficient way to modify state. For example, if we have two transactions each containing 5 lines of code that access shared state, with conventional solutions there would be 252 possible interleavings of the accesses to shared stat $(5 \times 2)!/5!^2$), which would have to be accounted for and locks added to protect them, with transactions there would be 2 possible dataflow graphs. Furthermore if we make an error in our design and use a variable through some back channel, this may cause a performance hit in the form of a bottleneck, but the transaction memory will prevent it causing a race condition.

5. The OpenStream extension to OpenMP

A key point of TERAFLUX is the compilation flow, which has been vastly remodeled to target the reference architecture. In particular, such compilation flow has been implemented as a front- and middle-end extension to GCC 4.7.1. Starting from a programming model which extends OpenMP to support streaming task directives, called OpenStream [46,27,47], the compiler is able to expand streaming task directives into dataflow threads and point-to-point communications. Programs written in higher level languages such as StarSs can be translated source-to-source to OpenStream using slightly modified implementations of their dependence resolver. The rationale for designing such streaming extension is motivated by the need to capture dataflow dependencies explicitly in a parallel language, by the quest for increased productivity in parallel programming, and by the strong evidence that has been gathered on the importance of pipeline parallelism for scalability and efficiency.

The OpenStream syntactic extension to the OpenMP language specification consists of two additional clauses for task constructs: the `input` and `output` clauses, both taking a list of items, describing the stream and its behavior. For example, within the body of a task, one can need to access each element of the stream one at a time (hence, the stream abbreviated form can be adopted), or multiple elements at a time through sliding windows (the forms adopting the << and >> stream operators are the most suitable). The syntax of the additional clauses (a) and an example of stream accessed via sliding window (b) is shown in Fig. 6. OpenStream supports dynamic voltage and frequency scaling under real-time constraints.

We conducted numerous performance evaluations with OpenStream. One key objective of the TERAFLUX project is to confirm the scalability advantages of a dataflow execution model. We study the scalability relative to the number of concurrent tasks created by the program, and relative to the number of cores. We selected the Gauss-Seidel benchmark for its dependence pattern highlighting the benefits of decoupled pipelines for load balancing and scalability. We consider three parallel versions: (1) the manually optimized OpenStream implementation, (2) the systematic conversion of the benchmark to OpenStream using a generic dependence resolver, and (3) the original StarSs benchmark.

The three versions expose the same degree parallelism and their execution unfolds into the same dynamic dependence graph.

The execution time of the three parallel versions as well as the sequential execution, running on 12 cores is shown in Fig. 7. The three parallel versions scale well, and show a slight advantage to dataflow execution with the OpenStream runtime. The reason for the performance difference is not related to the StarSs language or to the implementation of the benchmark. The default StarSs runtime behaves similarly to a token-based dataflow model: it needs to scan for ready tasks. More specifically, the StarSs runtime has a large shared data structure, the tree of regions, which is used to determine whether tasks are ready to execute. When the number of tasks increases, the time spent looking for ready tasks increases, as well as the contention on this data structure. In

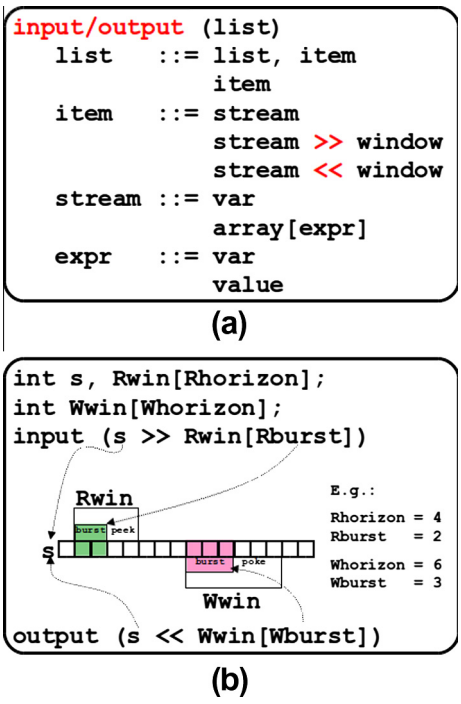

Fig. 6. Syntax for input and output clauses (a) and illustration of stream access through windows (b).

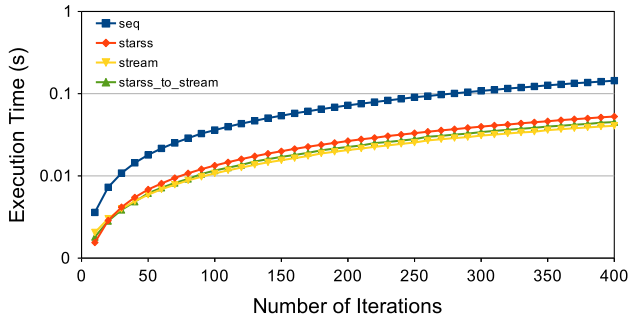

Fig. 7. Gauss-Seidel experiment for a 256 × 256 matrix, with 64 × 64 blocks. The benchmark was run on 12 cores. Four versions executed: OpenStream ('stream'); StarSs ('starss'); an OpenStream-StarSs combination ('starss_to_stream'); and a sequential version ('seq'), used as the baseline.

contrast, the target execution model of OpenStream is feed-forward dataflow, with a scheduler using one ready queue per core and work-stealing. This is possible because the OpenStream compiler generates code spending the extra effort at task creation to find the producer-consumer matching. The producers will then know when consumer tasks become ready, without any polling operation or any lookup in a shared data structure. Once a producer determines that one of its consumers has become ready, it adds it to its core-local, work-stealing ready queue. The systematic translation from the StarSs source code demonstrates that the performance bottlenecks are intrinsic to the runtime implementation and scheduling policy. The task-parallel language design and benchmark implementations can be transparently mapped to a more scalable, dataflow execution model, benefitting from its efficiency and scalability.

6. The TERAFLUX reference architecture

An important aspect of TERAFLUX is represented by the execution model and architecture framework [48] including hardware modules to support the execution model. The proposed template for the TERAFLUX architecture is shown in Fig. 8.

Besides using mostly off-the shelf parts, following the principle of "not reinventing the wheel", the architecture is designed to support an execution model that is a combination of fine- and corse-grain threaded dataflow models including DTA [4], DDM [49], StarSs [32]. In addition, the transactional support has been added to the dataflow model, which allow covering those applications that modify the shared state. Combining dataflow with transactions is a unique feature of this project.

In particular, Data-Driven Multithreading (DDM) [49] is one of the dataflow models studied in TERAFLUX. DDM is a multithreaded model that applies Dynamic Dataflow principles for communication among threads and exploits highly efficient control-flow execution within a thread. The core of DDM is the Thread Scheduling Unit (TSU, see Fig. 8) that provides the Data-Driven scheduling of the threads. DDM does not need traditional memory coherence because it enforces the single assignment semantics for data exchange among threads. Furthermore, it employs prefetching of input data before a thread is scheduled for execution by the TSU. DDM prefetching is deterministic and can be close to optimal because the TSU knows at any time which threads can be executed on which core and thus can initiate the necessary prefetching. DDM based processors can achieve high performance with simpler designs, as they do not need complex and expensive modules like out-of-order execution.

DDM was applied to three linear algebra HPC applications: Matrix Multiplication, LU decomposition and Cholesky decomposition. The scalability of DDM over a large number of cores was thus tested, and shows encouraging results [50]: DDM can handle the parallelization required for linear algebra applications for present and future multi- and many-core systems, and is thus a viable candidate for HPC.

A distributed version of DDM was also developed [51]. The main difference between single-node and distributed/multi-node DDM execution is the introduction of remote memory accesses resulting from producer and consumer threads running on different nodes. To this end, data forwarding is employed to the node where the consumer is scheduled to run. This is facilitated by supporting a Global Address Space (GAS) across all the nodes. A network interface unit has been implemented in the DDM-TSU to handle the low-level communication operations. In terms of the distribution of threads across the cores of the system nodes, this work explores a static scheme, in which the mapping is determined at compile time and does not change during the execution. The initial results on some kernel like matrix multiplication are very encouraging, leading to an almost linear speedup in configurations up to 32 x86_64 cores.

The TSU design has been also explored in the context of DTA [4]. In this case the TSus are organized in a 2-level hierarchy: one D-TSU at node level and one L-TSU besides each processing unit (standard core). Globally D-TSUs and L-TSUs form what is called the Distributed Thread Scheduler (DTS). In order to support the execution of DF-Threads, a minimalistic extension of the x86_64 ISA was designed, called T-Star (or T-∗) [52].

The key-points of the T-Star Instruction Set Extension (ISE) are: (i) it enables an asynchronous execution of threads, that will execute not under the control-flow of the program but under the dataflow of it; (ii) the execution of a DF-thread is decided by the Distributed Thread Scheduler, which monitors the availability of resources and enforces the higher level policies on power and performance constraints; (iii) it enables the usage and management by the DF-Threads of four types of memory regions as requested by the higher levels of the software to support 1-to-1 communication or Thread Local Storage (TLS), N-to-1 communication or Frame Memory (FM), 1-to-N communication or Owner Writable Memory

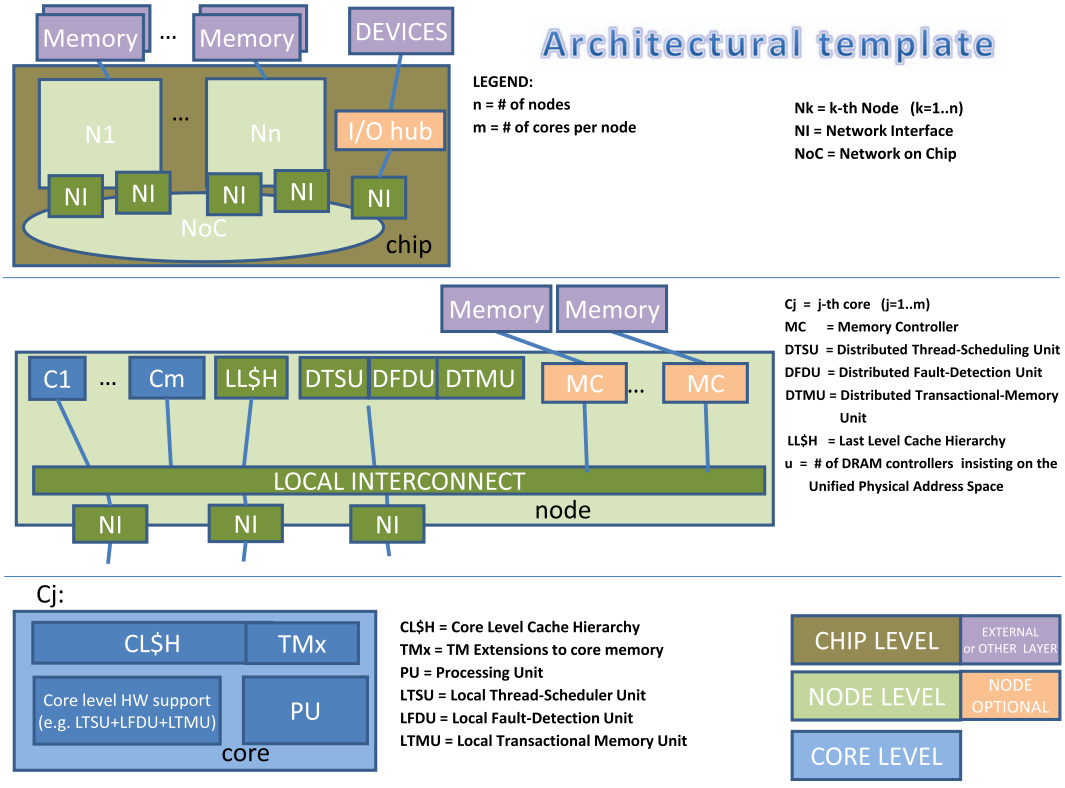

Fig. 8. TERAFLUX architecture template.

(OWM), and N-to-N communication or Transactional Memory (TM).

One feature of DF-Threads supported by the T-Star is their totally dynamic dataflow but without the burden of explicitely managing tokens [53]. The evaluation of this ISE has been carried out in the COTSon simulator: the initial programs were a recursive Fibonacci with input $n = 40$ and a Matrix Multiplication with matrix size 1024×1024 with the initial assumption of executing one instruction per cycle. The results of these test have demonostrated the full scalability of the TERAFLUX architecture up to 1024 cores organized as 32 nodes by 32 cores. The T-Star is available as part of COTSon at http://sf.net/p/cotson/code website.

7. Improving reliability by leveraging dataflow properties

The tera-scale level transistor integration capacity of future devices will make them orders of magnitude more vulnerable to faults. Without including mechanisms that dynamically detect and mask faults, such devices will suffer from uneconomic high failure rates. Four levels of reliability aspects are the focus of the TERAFLUX architecture, in order to assemble a reliable system out of unreliable components. These levels are (i) the cores; (ii) the nodes; (iii) the interconnection network; and (iv) the operating system.

At core and node level, we design specific units responsible for (i) monitoring the health state of the cores; and (ii) providing information to the hardware scheduler about the detected faults. We call such units Distributed Fault Detection Unit (D-FDU, operating at node-level) and Local Fault Detection Unit (L-FDU, at core-level). How the D-FDUs relate to a TERAFLUX node is shown in Fig. 9.

In TERAFLUX, the various D-FDUs detect faults by means of the Double Execution mechanism [54,31,55], a redundant execution scheme for DF-threads that we designed by leveraging the side-effect-free semantic of the dataflow execution. In particular, our mechanism duplicates the execution of each DF-Thread, and compares the results of both executions to check for correctness: L-FDUs are responsible for calculating a CRC-32 signature of both write sets, which will be sent to the D-FDU when the thread terminates. If the two signatures differ, a faulty execution is assumed, and the D-TSU is notified. Consequently, the results of the computation are discarded and the DF-threads may re-execute on different cores. The static dependency graph of a T∗ program (left) and the dynamically created dependency graph of the same program during a Double Execution run (right) is shown in Fig. 10. It can be seen that the original program first executes T0. Since this part of the program is sequential, the TERAFLUX runtime may exploit under-utilized cores for spatial redundant execution of T0. In case of a fault-free execution of T0, the synchronization counts of the successor threads are decremented, and the subsequent threads (T1 T1′), . . . , (Tn Tn′) can be executed.

At the interconnection level, efficient methods have been designed to localize faults within the network (router and link) [56–58]. The localization technique utilizes the knowledge of the

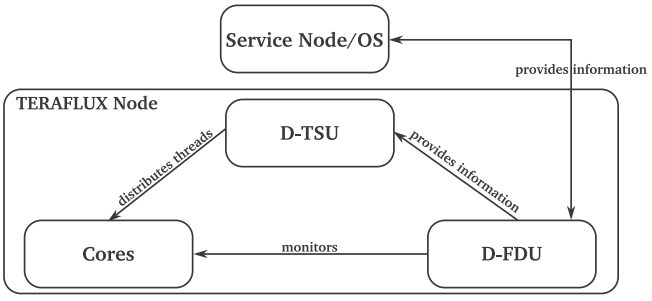

Fig. 9. Interaction between TERAFLUX Nodes, Service Node, Distributed-TSU (D-TSU) and Distributed FDU (D-FDU).

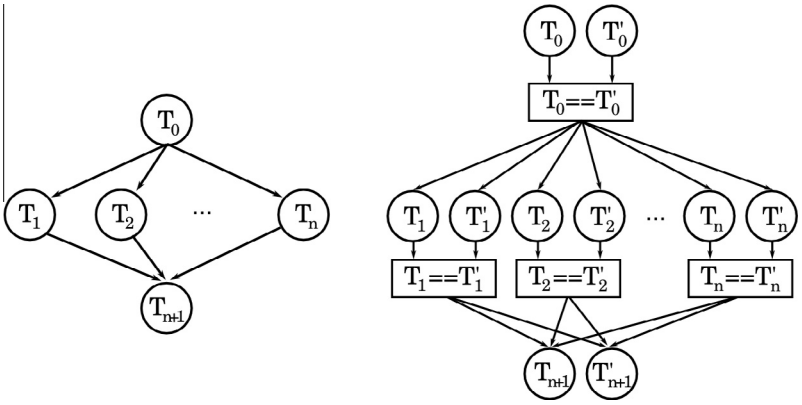

Fig. 10. Dependency graph for regular dataflow execution (left graph) and double execution (right graph).

existing heartbeat messages and extracts inherent information from them. For this, the knowledge of timing information gained from a special message sending pattern is combined with the message path information derived from the routing strategy. The timing pattern was originally designed to isolate heartbeat messages and avoid collisions between them. The pattern regulates the network access for the L-FDUs and is based on the Time Division Multiple Access (TDMA) concept for concurrent media access in computer networks or real time bus systems. In conjunction with the Quality of Service, where heartbeat messages are transferred with the highest priority, it supports a precise estimation of the arrival time of all heartbeat messages at the D-FDU. Supposing that a message was delivered with a delay, indicated by an increased hop count, the receiving D-FDU can conclude that the message was transmitted over a bypass due to a faulty network element.

The routing information is then used to determine where the faulty network component is located. Since the D-FDU investigates an unusual timing behavior of one or more heartbeat messages, the path of these messages is marked as suspicious. Therefore, the D-FDU is holding a network status matrix, which encodes the fault information of the NoC. The suspicious path elements in this matrix are set by incrementing each entry by "1" for each suspicious component. Each heartbeat message arriving in time at the D-FDU ensures that the values corresponding to the message's path are decremented within this matrix. In that manner, a value of smaller than "1" stands for a fault-free component. With this process of elimination, the D-FDU is able to locate faulty network elements.

Finally, the D-FDUs forward the gathered node health states to the operating system to provide additional information for global scheduling decisions.

8. The common evaluation platform

The TERAFLUX project relies on a common evaluation platform [9,59] that is used by the partners with two purposes: (i) evaluate and share their research by using such integrated, common platform, and (ii) transfer to the other partners the reciprocal knowledge of such platform.

The common platform includes not only the COTSon simulator, but it also encompasses the compiler that is being developed in the project, as well as support tools (e.g., McPAT [60] for power estimation) and libraries (for StarSs region matching) that we integrated to meet our research needs.

An overall picture that highlights what the software sees—as a simulated machine—is shown in Fig. 11. The relevant point is that the software should not look inside the COTSon simulated machine, or make any assumption about the developing architecture: the exact purpose is to decouple the process of software design and hardware design (while keeping a "contract" between them) [61,62].

Therefore the simulation software exposes a number of virtual processors where the guest software can run unmodified (called VCPUs). From the software point of view all these VCPUs could be both considered as full x86_64 virtual machines or as simple "x86_64 ISA cruncher" (or "Auxiliary Cores"). The simulator may expose the latter capability to the Operating System (OS), but for the sake of generality the application software should not presume the availability of any OS-service: each VCPU is just a bare machine. COTSon, on the other side, can implement any virtualization trick to make this illusion becoming available.

One or more VCPUs assume the role of "Service Cores" (e.g., the *k*th) and runs a guest Linux OS that provides the necessary support to load both TERAFLUX Applications (TFX APPS for short) and run LEGACY APPS (such as the Oracle DBMS). The only support required by the OS is a modification of the internal scheduler (this could be provide as a "driver" in the future) in order to set the high level policies for the TSUs. The TSUs will enforce such policies and take care of the global bookkeping of the various types of threads (DF-Threads, Legacy-Threads (such as from legacy applications),

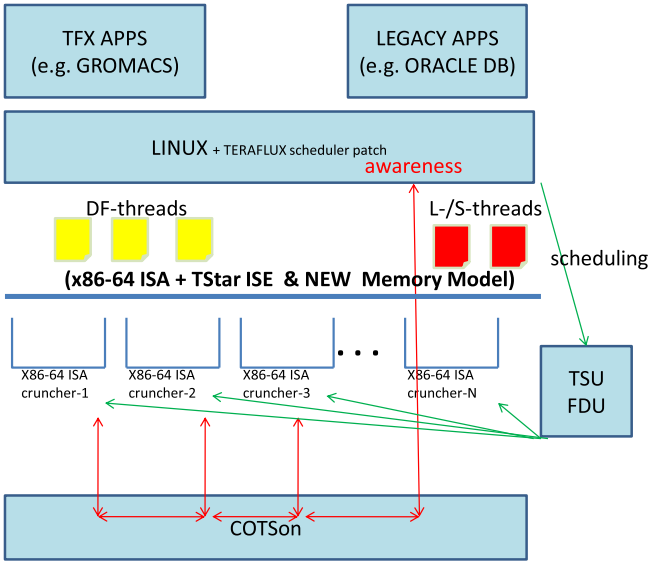

Fig. 11. Overall picture of the "simulator illusion". A number *n* of VCPUs can be used as "workers" or "x86_64 cruncher" or "Auxiliary Cores" or "Service Cores"; a generic *k*th VCPU can be used as service core. L- and S-threads represent Legacy and System Threads, that our system is able to execute.

System-Threads (supporting OS services on the Service Core — respectiely DF-, L-, S-Threads).

We extended the COTSon platform in order to support the TERAFLUX dataflow execution models (both DDM and T∗). In particular, we added the full support for the T∗ extension to the x86_86 ISA, by implementing a model for the TSU. We also added a fault-injection model for evaluating the overhead introduced by the Double Execution mechanism, which was also modeled with the FDU. Finally, we extended the platform in order to pass from a cluster-based view of the target teradevice system, to a many-nodes-per-chip one, by realizing a communication mechanism via the host shared memory, considering appropriate timing model [63]. More recent steps deal with the further refinement of the T∗ Instruction Set Extension and its integration with the Transactional Memory.

9. The Codelet model

As a further extension of the TERAFLUX program execution model, the University of Delaware joined our project bringing its expertise on the codelet model. The Codelet Model [6] is a hybrid Von Neumann-dataflow execution model, aimed at providing a fine-grain parallel execution model. Its quantum of computation is called a codelet. A codelet (pictured in Fig. 12) is an event-driven sequence of machine instructions, which run until completion. Foremost among those events is data availability, which is the prime reason to trigger the execution of a codelet (which we call firing). All events are explicitly expressed when defining the codelets. Besides the required data (following dataflow semantics), events on which a codelet may wait until it is fired include bandwidth requirements, core frequency (including a given maximal temperature or power expenditure), etc. Codelets are expected to be generated by a compiler. Previous experience with the codelet model's ancestor, EARTH [64], have shown that automatic partitioning programs into threads that follow dataflow semantics is indeed possible [65].

The codelet execution model relies on an Abstract Machine Model (AMM). It features a hierarchical topology, as well as a heterogeneous architecture. From a high-level point of view the codelet AMM is rather close to the TERAFLUX architectural template. The important part is located at the chip level: the scheduling part is delegated to a dedicated unit (the scheduling unit, equivalent of the TSU in the TERAFLUX architectural template), while the computational part is performed by the computation units (which are called cores in TERAFLUX). As a principal scheduling quantum, a codelet, once allocated and scheduled to a core, keeps the computation unit usefully busy, and cannot be preempted (however it can voluntarily yield, provided that more than one codelet context can be held within the same core—thus allowing for overhead-less context switches). One feature of the codelet execution is the efficient support of a non-preemptive event-driven thread model. If the system software deems it necessary, it can clock-gate (or even power-gate) selected cores. The codelets running on those cores must thus be suspended for the duration of the core suspension—and subsequently resumed once the TSU it depends on decides to turn the core on again. Codelets running on cores that are power-gated must be restarted (either on the same core or on another).

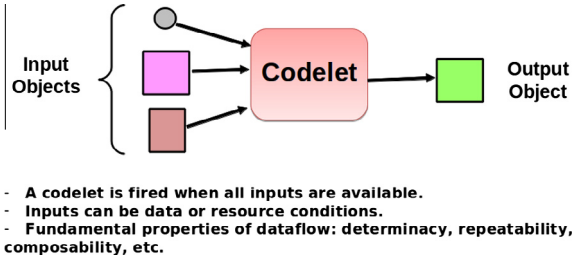

Fig. 12. The Codelet: a Fine-Grain Piece of Computation. A codelet is fired when all inputs are available. Inputs can be data (square inputs) or resource conditions (gray circle).

The codelet model features asynchronous functions, called Threaded Procedures. They are called in a control-flow manner, and act as containers for codelet graphs. A threaded procedure (TP) features a frame which is shared by all the codelets. Following the precepts of dataflow, when possible, most data is written in a "write once, read many times" manner: data is produced by a given codelet, and consumed by one or more depending codelets. Threaded procedures provide a second level of parallelism, as well as a locality constraint: all codelets contained within a given TP must run on the same group of cores within a node. Therefore, while there is nothing to prevent the grouping of unrelated codelets within a given TP, locality requirements tend to ensure that TPs are containers for a logical grouping of codelets, much like traditional functions are logical groupings of instructions. The availability of the TP frame to all its contained codelets implies that all codelets can read and write all its data: two codelets executing in parallel may potentially read and/or write to the same frame location simultaneously. Therefore a memory consistency model must be provided to handle those cases.

The codelet memory model is based on Location Consistency (LC) [66]. LC does not require a global ordering of memory operations on the same memory location visible to all processors. Consequently, a memory model based on LC should provide better scalability than other existing cache-coherent based models and protocols.

We have provided an implementation of the Codelet model as a runtime system: the Delaware Adaptive Run-Time System (DARTS) [67]. It is written in C++, and can run on any POSIX-compliant system. In addition, we have ported DARTS to the TERAFLUX simulator, thus taking advantage of the TERAFLUX instruction set extension to schedule dataflow threads. The codelet and DF-Thread models are sufficiently close that we can try to find a converging path toward a new dataflow-inspired execution model, of which the port of DARTS on the TERAFLUX machine (the COTSon simulator) is a first significant step. Codelets are mapped to DF-Threads, thus allowing DARTS to make use of the TSU on COTSon. We are also studying different percolation techniques for teradevices. Percolation [68] is a mechanism that determines how code and/or data should be located, and where, on a given machine. It also takes into account the bandwidth availability. Its goal is to guarantee as much locality as possible for the on-going computation. Other research is currently under way to combine the Codelet model with streaming. Preliminary results are encouraging [69,70].

Other projects seem to move along similar directions [71,72].

10. Conclusions

We presented TERAFLUX, a Future Emerging Technology Large-Scale Project funded by the EU. TERAFLUX is at the forefront of major research challenges such as programmability, manageable architecture design, and reliability of many-core or 1000+ cores chips. We described the project's transformation hierarchy and its major scientific contributions. These contributions include scalable parallel applications, programming models for large-scale systems exploiting the dataflow principles, compiler techniques and tools to harness a dynamic, thread-level dataflow execution model, fault-detection and -tolerance techniques, the actual architecture, and the simulation infrastructure needed for the evaluation of

the proposed research. The preliminary results demonstrate solid performance scalability and reliable execution over unreliable components. The TERAFLUX architecture builds on top of classical microarchitecture principles for the individual cores and their closest local memories, and combines a large number of them with simple modules such as the Thread Scheduling Units and Fault Detection Units. Among the notable contributions, StarSs-inpired dependent tasking construct have been integrated into the OpenMP4 specification, and the project released a simulator able to perform experiments with more the 1000 general purpose cores and full system simulation (COTSon).

Acknowledgements

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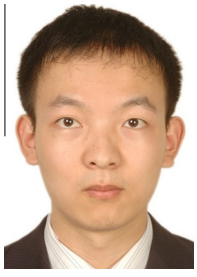

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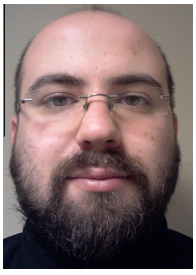

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