Extending Performance and Reliability via Modular FPGA Clusters

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***Abstract*— As the number of transistors per computing system is ever-increasing, so are the fault rates. This issue may be critical also in the area of embedded systems, as they may work in mission-critical conditions and in contexts where they may be subject to several sources of faults. We propose to provide a further dimension of flexibility by federating the capabilities of several separated FPGA-based independent systems, so as to provide a more resilient system that can also improve the performance by simply joining more systems via an inexpensive and simple high-speed interconnect.**
Differently, from traditional checkpointing or lock-stepping, we foresee the possibility of relying on a disciplined data flow among the application threads. The underlying execution model is known as dataflow-threads (DF-threads) and the fault-detection extension of this model allows to achieve a resilient execution of an application while faults are affecting the system. In the proposed implementation, the execution time gracefully degrades as the number of faults increases, without the need for global checkpointing and without interrupting the application execution. The technique has been evaluated on a full-system x86-64 simulator with encouraging results and an FPGA-based implementation is under development.

Keywords- Reliability, Reconfigurable Computing, Dataflow, Multi-threading, Distributed System, FPGA

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About author

Roberto Giorgi *is an Associate Professor at the University of Siena, Italy (qualified for Full Professorship). He received his PhD in Computer Engineering and his Master in Electronics Engineering, Summa cum Laude both from University of Pisa, Italy. He has been coordinator of a FET EU project (TERAFLUX), and of an H2020 project (AXIOM), Workpackage leader of the Embedded Reconfigurable Architecture project, deputy steering committee member in HiPEAC, participating in SARC (Scalable ARChitectures). He took part in ChARM project, developing software for performance evaluation of ARM-processor based embedded systems with cache. He is an author of more than 130 scientific papers. His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization, Reconfigurable Computing. He is a Lifetime member of ACM and a Senior member of the IEEE, IEEE Computer Society.*

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