

GLUON, The High-Speed Inexpensive and Easy Interconnect Solution

Amin Sahebi^{*†,1}, Roberto Giorgi^{*,2}

^{*} *Università degli Studi di Siena, Siena, Italy*

[†] *Università degli Studi di Firenze, Firenze, Italy*

ABSTRACT

Heterogeneous systems are one of the most discussed architectures in computer science. Their capabilities have provided many good features for researchers to use this kind of structure in their state-of-the-art works. Heterogeneous systems are flexible, cost-efficient, and well-supported by communities. They are widely used in artificial intelligence, automotive, IoT, and embedded applications. Moreover, there is also a challenge to have a sufficient, cost-efficient, and flexible structure to use heterogeneous systems. In this work, we present the GLUON board, which is capable of using serial transceivers in Xilinx Ultra-scale+ structure and facilitates using GTH transceivers in high rate data transfer applications, the possible solution would be a high data rate cluster network based on Zynq Ultra-scale+ MPSoCs, which can easily deploy a multi-node, multi-code structure in reasonable cost.

KEYWORDS: Serial Transceivers, Xilinx Ultra-scale+, Heterogenous structure.

1 Introduction

In recent years, there are some works to introduce a heterogeneous platform such as AXIOM [GKP19a], which can provide flexible infrastructure for AI applications as well discussed in [GKP19b]. However, there was a need to exploit all serial transceivers of Xilinx Ultra-scale+, plus, can also capable of carrying fully operating support with a sufficient amount of memory. We designed the GLUON board, which can provide all these requirements. As can be seen in Fig.1, the idea is to provide necessary elements to build a FPGA based cluster to accelerate applications such as AI, IoT, automotive and computing applications [KPG18, SVG19, AS12]. The structure can work as ultrafast communication network like Infiniband. The main difference and advantage is there is no need for any external switch and the cost of network is reasonable because in our structure we use just USB-C receptacles to connects Nodes with USB-C cables, which are inexpensive and easy to maintenance and handle in complicated topologies. In this structure, the worker Nodes Fig. 1, , can be connected to each

¹E-mail: sahebi@diism.unisi.it

²E-mail: giorgi@dii.unisi.it

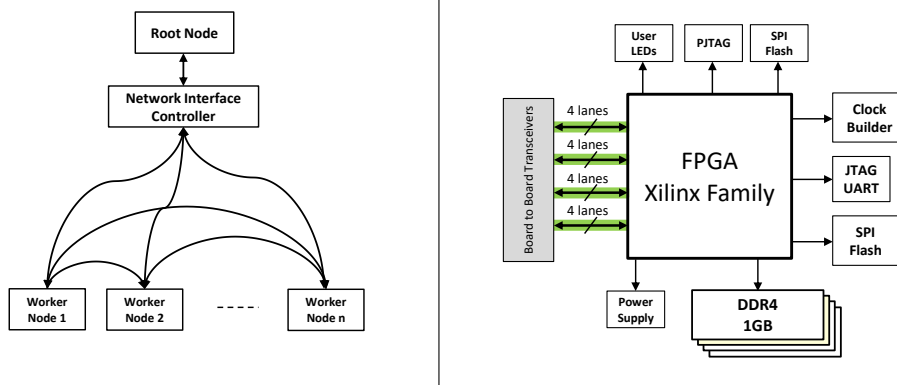


Figure 1: The overview of the network, based on GLUON interconnects

other and can receive orders by the Root node. The connection between each two Nodes is up to 16 Gb/s and the topology of the network can be define by the user and depends on the applications. This infrastructure, facilitate the road to have a distributed system, which is applicable to develop and test many interesting ideas. The manufactured Gluon board is shown in Fig.3, which is carrying Xilinx XCZU9EG Xilinx ultrascale+ module show in Fig. 2.



Figure 2: The Xilinx XCZU9EG Xilinx Ultrascale+ module

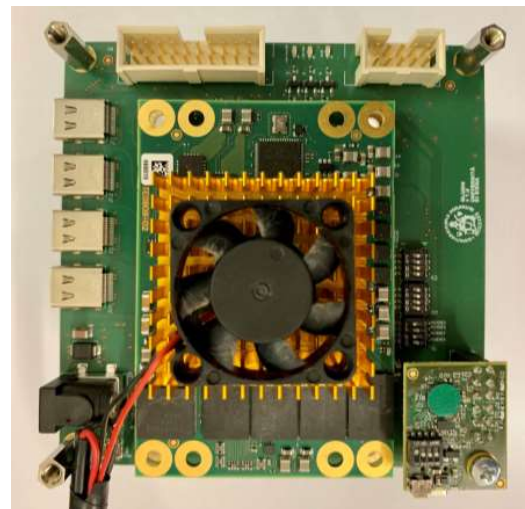


Figure 3: The manufactured GLUON board plus the Xilinx XCZU9EG module.

2 Conclusion and future works

We designed and presented the first version of the GLUON board, which provides necessary elements to fully exploit Giga Transceivers of Xilinx Ultrascale+ modules. This structure is cost-effective, reliable, and flexible, a different number of modules of Xilinx MPSoCs can embark on this carrier board. The speed rate of GTH transceivers has been calculated by a

Specifications	Description
PL GT Transceivers	8 Differential Pair in total, 16.3 Gb/s
SD Card	Boot the Operating System
JTAG/UART header	
10 Pin I2C header for "Silabs" Clock Builder Field Programmer	To configure the Si5345 Clock Generator
Done, Error/Status LEDs	
PS I/O loopbacks	
PL I/O loopbacks	

Figure 4: Gluon board Specification Table

running full Ubuntu AXIOM software stack as mentioned [AAB⁺16]. For the future work, there might be some area of work that, we can add some useful features to GLUON board, that can cover more area of computing science some applications like FFT [LV19], [KPG18], and also RISC-V applications by using the proper modules from Xilinx products can be achievable by a significantly reasonable cost.

References

- [AAB⁺16] Carlos Alvarez, Eduard Ayguade, Jaume Bosch, Javier Bueno, Artem Cherkashin, Antonio Filgueras, Daniel Jimenez Gonzalez, Xavier Martorell, Nacho Navarro, Miquel Vidal, Dimitris Theodoropoulos, Dionisios N Pnevmatikatos, Davide Catani, David Oro, Carles Fernandez, Carlos Segura, Javier Rodriguez, Javier Hernando, Claudio Scordino, Paolo Gai, Pierluigi Passera, Alberto Pomella, Nicola Bettin, Antonio Rizzo, and Roberto Giorgi. The axiom software layers. *Microprocessors and Microsystems*, 47:262 – 277, 2016.
- [AS12] Amin Sahebi Ali Soleimani. Using neural networks to predict road roughness. *Journal of Solid and Fluid Mechanics*, 2:63 – 69, 2012.
- [GKP19a] R. Giorgi, F. Khalili, and M. Procaccini. Axiom: A scalable, efficient and reconfigurable embedded platform. In *IEEE Proc. Design, Automation and Test in Europe (DATE)*, pages 1–6, Florence, Italy, Mar. 2019.
- [GKP19b] R. Giorgi, Farnam. Khalili, and Marco Procaccini. Translating timing into an architecture: The synergy of cotson and hls (domain expertise – designing a computer architecture via hls). *Hindawi - International Journal of Reconfigurable Computing*, Dec. 2019.
- [KPG18] F. Khalili, M. Procaccini, and R. Giorgi. Reconfigurable logic interface architecture for cpu-fpga accelerators. In *HiPEAC ACACES-2018*, pages 1–4, Fiuggi, Italy, July 2018. poster.
- [LV19] R. Giorgi L. Verdoscia, A. Sahebi. A data-flow methodology for accelerating fft. *The 8th Mediterranean Conference on Embedded Computing - MECO*, 2019.

- [SVG19] Amin Sahebi, Lorenzo Verdoscia, and Roberto Giorgi. A data-flow approach to accelerate real-valued fast fourier transform. In *HiPEAC ACACES-2019*, pages 155–158, Fiuggi, Italy, July 2019. poster.